## REMARKS

Applicant respectfully requests further examination and reconsideration in view of the above amendments and the comments set forth fully below. Claims 1-31 were pending. Within the Office Action, claims 1, 15 and 18 have been rejected and claims 2-14, 16, 17 and 19-31 have been objected to. Applicant has amended claims 1, 2, 15, 16, 18 and 19. Claims 1-31 are now pending.

### Rejections Under 35 U.S.C. § 103

Within the Office Action, claims 1, 15 and 18 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,663,989 to Fobbester (hereinafter "Fobbester") in view of U.S. Patent No. 5,960,046 to Morris et al. (hereinafter "Morris"). The Applicant respectfully disagrees with this rejection. Fobbester teaches frequency differences between transmitter and receiver in a frequency modulated digital radio transmission system which give rise to DC offsets at the output of the demodulator are countered for any one data transmission by establishing a frequency controlling or DC level controlling signal during a preamble sequence having a known constant DC component, such as the sequence 10101 - - - used for clock or data synchronization, and retaining that controlling signal substantially unaltered for use during the remainder of that data transmission. [Fobbester, Abstract].

As recognized by the Office Action, Fobbester does not teach a control signal being applied to the DC level set circuit to place the DC level set circuit into operation. Fobbester also does not disclose a preamble detector configured to receive the input signal and to provide a preamble signal, in that figure 4, reference 12 does not teach this element as is stated in the Office Action. Furthermore, the Applicant respectfully submits that Fobbester does not disclose a four bit delay line for detecting and for holding the preamble portion of the signal.

Morris teaches a selection diversity system and method for use in a TDMA (time division multiple access) radio system, particularly suited for DECT (Digital Enhanced Cordless Telephone) applications, in which a single receiver makes a performance measurement on each of two antennas in sequence during the beginning of a received data burst, the beginning of the burst being determined by a timing signal fed back from a previous burst. A slicing level used in the receiver to perform threshold detection is continuously improved during the measurements of the two antennas, but held while switching between the antennas. The previously unused antenna is measured first to minimize the likelihood of having to perform two antenna switches. [Morris, Abstract]. Accordingly, neither Fobbester, Morris nor their combination teach a control signal being applied to the DC level set circuit to place the DC level set circuit into operation, a

preamble detector configured to receive the input signal and to provide a preamble signal or a four bit delay line for detecting and for holding the preamble portion of the signal.

In contrast to the teachings of Fobbester, Morris and their combination, the data recovery algorithm for implementation in a radio transmitter or receiver includes a direct current level setting circuit with a preamble detector which will establish a threshold for a simplified decision simplified equalizer slicer that improves receiver performance in a feedback manner by utilizing an analog comparator, a one symbol long one bit resolution delay line and a summing junction. As described above, neither Fobbester, Morris nor their combination teach the feature of a control signal being applied to the DC level set circuit to place the DC level set circuit into operation, a preamble detector configured to receive the input signal and to provide a preamble signal or a four bit delay line for detecting and for holding the preamble portion of the signal.

The independent claim 1 is directed to a circuit in a wireless receiver for receiving an input signal from a transmitter, the input signal including a preamble portion, a unique word portion and a data portion comprising a preamble detector configured to receive the input signal and to provide a preamble signal where the preamble signal is active during the preamble portion of the input signal and inactive during all portions of the input signal other than the preamble portion, a DC level set circuit configured to receive the preamble signal, the input signal including the preamble portion, the unique word portion and the data portion and to receive the control signal and to provide a level set signal, a data slicer circuit coupled with the DC level set circuit to receive the level set signal and to provide the output signal and a four bit delay line for detecting and for holding the preamble portion of the signal. As described above, neither Fobbester, Morris nor their combination teach the feature of a control signal being applied to the DC level set circuit to place the DC level set circuit into operation, a preamble detector configured to receive the input signal and to provide a preamble signal or a four bit delay line for detecting and for holding the preamble portion of the signal. For at least these reasons, the independent claim 1 is allowable over the teachings of Fobbester, Morris and their combination.

The independent claim 15 is directed to a method of receiving an input signal and a control signal and providing an output signal, the input signal including a preamble portion, a unique word portion and a data portion comprising receiving the input signal with a preamble detector, providing a preamble signal where the preamble signal is active during the preamble portion of the input signal and inactive during all portions of the input signal other than the preamble portion, receiving the preamble signal from the preamble detector, the input signal and the control signal with a DC level set circuit, providing a level set signal with the DC level set circuit, receiving the level set signal from the DC level set circuit with a data slicer circuit and

providing the output signal with the data slicer circuit, wherein the preamble detector provides the preamble signal to the DC level setting circuit when a four bit delay line detects the preamble portion of the input signal. As described above, neither Fobbester, Morris nor their combination teach the feature of applying a control signal to the DC level set circuit to place the DC level set circuit into operation or providing a preamble signal, wherein the preamble detector provides the preamble signal to the DC level setting circuit when a four bit delay line detects the preamble portion of the input signal. For at least these reasons, the independent claim 15 is allowable over the teachings of Fobbester, Morris and their combination.

The independent claim 18 is directed to a circuit for receiving an input signal and a control signal and providing an output signal, the input signal including a preamble portion, a unique word portion and a data portion comprising means for receiving the input signal with a preamble detector, means for providing a preamble signal where the preamble signal is active during the preamble portion of the input signal and inactive during all portions of the input signal other than the preamble portion, means for receiving the preamble signal from the preamble detector, the input signal and the control signal with a DC level set circuit, means for providing a level set signal with the DC level set circuit, means for receiving the level set signal from the DC level set circuit with a data slicer circuit, means for providing the output signal with the data slicer circuit and means for detecting and holding the preamble portion of the input with a four bit delay line. As described above, neither Fobbester, Morris nor their combination teach means for applying a control signal to the DC level set circuit to place the DC level set circuit into operation, means for providing a preamble signal or means for detecting and holding the preamble portion of the input with a four bit delay line. For at least these reasons, the independent claim 18 is allowable over the teachings of Fobbester, Morris and their combination.

**Allowable Subject Matter**

Within the Office Action, claims 2-14, 16-17 and 19-31 have been objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. As discussed above, claims 1, 15 and 18 are allowable over the teachings of Fobbester, Morris and their combination. Accordingly, the dependent claims 2-14, 16, 17 and 19-31 are all also allowable as being dependent on an allowable base claim.

For the reasons given above, Applicant respectfully submits that the claims are now in a condition for allowance, and allowance at an early date would be appreciated. Should the Examiner have any questions or comments, they are encouraged to call the undersigned at (408) 530-9700 to discuss the same so that any outstanding issues can be expeditiously resolved.

Respectfully submitted,
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Dated: July 16, 2004

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CERTIFICATE OF MAILING (37 CFR§ 1.8(a))

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being deposited with the U.S. Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to the: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450

HAVERSTOCK & OWENS LLP.

Date: 7-16-04 By: